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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/434,299	11/05/1999	JAMES A. JOHANSON	JOHANSON79-3	3784

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EXAMINER
ANYA, CHARLES E

ART UNIT	PAPER NUMBER
2126	

DATE MAILED: 07/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/434,299	JOHANSON ET AL.	
	Examiner	Art Unit	
	Charles E Anya	2126	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1/ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 are pending in this application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 4 and 6 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. 3,924,245 to Eaton et al. in view of U.S. Pat. No. 5,608,873 to Feemster et al.

4. As to claim 1, Eaton teaches a shared memory processor-to-processor mailbox between at least two processors ("...two separate processing unit..." Col. 6 Ln. 43 – 54), comprising: a shared memory accessible by a first processor and a second processor (Microprogram Store 11 Col. 6 Ln. 43 – 54), a first mailbox portion (Stack 26/Stack 25 Col. 4 Ln. 7 – 22) and a second mailbox portion both being defined at least in part over common memory addresses (Microgrogram Store 11 Col. 4 Ln. 7 – 22), said first mailbox portion starting at a low physical address end of said shared memory, and addressably filling upward through to a highest physical address of said common memory ("...extend upwards..." Col. 4 Ln. 7 – 22), said second mailbox portion starting

at said high physical address end of said shared memory, and addressably filling downward through to said lowest physical address of said common memory ("...extends downwards..." Col. 4 Ln. 7 – 22).

5. Eaton is silent with respect to said shared memory including a first mailbox portion to pass data from said first processor to said second processor, and a second mailbox portion to pass data from said second processor to said first processor and the first processor having write access to the first mailbox portion and not to the second mailbox portion.

6. Feemster teaches said shared memory including a first mailbox portion to pass data from said first processor to said second processor, and a second mailbox portion to pass data from said second processor to said first processor (figure 2 Col. 5 Ln. 45 – 67, Col. 6 Ln. 16 – 30) and the first processor having write access to the first mailbox portion and not to said second mailbox portion ("...not write..." Col. 4 Ln. 4 – 16).

7. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Feemster and Eaton because the teaching of Feemster would improve the system of Eaton by providing data passing scheme between processors and read-write access to a mailbox (Col. 4 Ln. 4 – 16).

8. As to claim 2, Feemster teaches the shared memory processor-to-processor mailbox between at least two processors according to claim 1, wherein said second processor has write access to said second mailbox portion and not said first mailbox portion ("...write-access..." Col. 4 Ln. 4 – 16).

9. As to claim 3, Feemster teaches to the shared memory processor-to-processor mailbox between at least two processors according to claim 1, wherein said first processor has read access to said first mailbox portion and not to said second mailbox portion ("...read-access..." Col. 4 Ln. 4 – 16).

10. As to claim 4, Feemster teaches with the shared memory processor-to-processor mailbox between at least two processors according to claim 3, wherein said second processor has read access to said first mailbox portion to said second mailbox portion ("...read-access..." Col. 4 Ln. 4 – 16).

11. As to claim 6, Feemster teaches the shared memory processor-to-processor mailbox between at least two processors according to claim 1, wherein said first processor has read access from both said first mailbox portion and said second mailbox portion while having write access to said first mailbox portion and not to said second mailbox portion ("...read-access...write..." Col. 4 Ln. 4 – 16).

12. As to claim 7, Feemster teaches the shared memory processor-to-processor mailbox between at least two processors according to claim 6, wherein said second processor has read access from both said first mailbox portion and said second mailbox portion while having write access to said second mailbox portion and not to said first mailbox portion ("...read-access...write..." Col. 4 Ln. 4 – 16).

13. As to claim 8, Eaton teaches a method of utilizing a shared memory as a mailbox between two processors ("...two separate processing unit..." Col. 6 Ln. 43 – 54), comprising: providing a contiguous block of shared memory (Microprogram Store 11 Col. 6 Ln. 43 – 54), allowing said first direction messages to utilize a dynamically allocated shared central portion of said shared memory addressably filling through to said second physical address end ("...extend upwards..." Col. 4 Ln. 7 – 22), and allowing said second direction messages to utilize said dynamically allocated shared central portion of said shared memory addressably filling through to said first physical address end ("...extends downwards..." Col. 4 Ln. 7 – 22).

14. Eaton is silent with reference to allocating first direction messages passed from a first processor to a second processor to a first physical address end of said shared memory, allocating second direction messages passed from said second processor to said first processor to a second physical address end of said shared memory opposite said first physical address end.

15. Feemster teaches allocating first direction messages passed from a first processor to a second processor to a first physical address end of said shared memory, allocating second direction messages passed from said second processor to said first processor to a second physical address end of said shared memory opposite said first physical address end (figure 2 Col. 5 Ln. 45 – 67, Col. 6 Ln. 16 – 30).

16. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Feemster and Eaton because the

teaching of Feemster would improve the system of Eaton by providing data passing scheme between processors and read-write access to a mailbox (Col. 4 Ln. 4 – 16).

17. As to claim 9, Eaton teaches the method of utilizing a shared memory as a mailbox between two processors according to claim 8, further comprising: assigning a minimum length to said first physical address end (Stack 26 Col. 4 Ln. 7 – 23).

18. As to claim 10, Eaton teaches the method of utilizing a shared memory as a mailbox between two processors according to claim 9, further comprising: assigning a minimum length to said second physical address end (Stack 25 Col. 4 Ln. 7 – 23).

19. As to claim 11, Eaton teaches the method of utilizing a shared memory as a mailbox between two processors according to claim 8, further comprising: reallocating a portion of a minimum length of said first physical address end of said shared memory to enlarge a size of said dynamically allocated central portion utilized by said first processor (see figure 2, Col. 4 Ln. 7 – 22).

20. As to claim 12, Eaton teaches the method of utilizing a shared memory as a mailbox between two processors according to claim 11, further comprising: reallocating a portion of a minimum length of said second physical address end of said shared memory to enlarge a size of said dynamically allocated central portion utilized by said second processor (see figure 2, Col. 4 Ln. 7 – 22).

21. As to claim 13, Eaton teaches an apparatus for utilizing a shared memory as a mailbox between two processors ("...two separate processing unit..." Col. 6 Ln. 43 – 54), comprising: means for allowing said first direction messages to utilize a dynamically allocated shared central portion of said shared memory addressably filling through to said second physical address end ("...extend upwards..." Col. 4 Ln. 7 – 22), and means for allowing said second direction messages to utilize said dynamically allocated shared central portion of said shared memory addressably filling through to said first physical address end ("...extends downwards..." Col. 4 Ln. 7 – 22).

22. Eaton is silent with reference to shared memory means for providing a contiguous block of shared memory means for allocating first direction messages passed from a first processor to a second processor to a first physical address end of said shared memory means for allocating second direction messages passed from said second processor to said first processor to a second physical address end of said shared memory opposite said first physical address end.

23. Feemster teaches shared memory means for providing a contiguous block of shared memory means for allocating first direction messages passed from a first processor to a second processor to a first physical address end of said shared memory means for allocating second direction messages passed from said second processor to said first processor to a second physical address end of said shared memory opposite said first physical address end figure 2 Col. 5 Ln. 45 – 67, Col. 6 Ln. 16 – 30).

24. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Feemster and Eaton because the teaching of Feemster would improve the system of Eaton by providing data passing scheme between processors and read-write access to a mailbox (Col. 4 Ln. 4 – 16).

25. As to claim 14, Eaton teaches the apparatus for utilizing a shared memory as a mailbox between two processors according to claim 13, further comprising: means for assigning a minimum length to said first physical address end (Stack 26 Col. 4 Ln. 7 – 23).

26. As to claim 15, Eaton teaches the apparatus for utilizing a shared memory as a mailbox between two processors according to claim 14, further comprising: means for assigning a minimum length to said second physical address end (Stack 25 Col. 4 Ln. 7 – 23).

27. As to claim 16, Eaton teaches the apparatus for utilizing a shared memory as a mailbox between two processors according to claim 14, further comprising: reallocating a portion of a minimum length of said first physical address end of said shared memory to enlarge a size of said dynamically allocated central portion utilized by said first processor (see figure 2, Col. 4 Ln. 7 – 22).

28. As to claim 17, Eaton teaches the apparatus for utilizing a shared memory as a mailbox between two processors according to claim 16, further comprising: means for reallocating a portion of a minimum length of said second physical address end of said shared memory to enlarge a size of said dynamically allocated central portion utilized by said second processor (see figure 2, Col. 4 Ln. 7 – 22).

29. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. 3,924,245 to Eaton et al. in view of U.S. Pat. No. 5,608,873 to Feemster et al. as applied to claim 1 above, and further in view of U.S. Pat. No. 5,802,351 to Frampton.

30. As to claim 5, Eaton is silent with respect the shared memory processor-to-processor mailbox between at least two processors according to claim 1, wherein said shared memory is a dual port random access memory.

31. Frampton teaches the shared memory processor-to-processor mailbox between at least two processors according to claim 1, wherein said shared memory is a dual port random access memory (Dual Port Random Access Memory Device 31 Col. 3 Ln. 18 – 26).

32. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Frampton, Eaton and Feemster because the teaching of Frampton would improve the system of Eaton as modified by Feemster by buffering data transferred between a MCU and DSP (Col. 3 Ln. 20 – 26).

Response to Arguments

33. Applicant's arguments filed 6/01/04 have been fully considered but they are not persuasive.

34. In the remarks, Applicant argued in substance that (1) the Eaton prior art reference teaches the use of memory by a single processor and as such the memory is not shared; (2) that the Eaton prior art reference does not teach passage of data from one processing unit to another processing unit; (3) that there is no motivation to combine the teachings of Eaton and Feemster; (4) that the combination of Eaton and Feemster fails to teach first and second mailbox portions both defined in part over common memory addresses and the first mailbox addressably filling upward through the a highest physical address of the common memory and second mailbox addressably filling downward through to a lowest physical address of the common memory.

35. Examiner respectfully traverses Applicant's remarks:

A. As to point (1), as Applicant rightfully acknowledged the Eaton prior art reference, though in the very last paragraph, discloses multiple processors that share common memory, thus negating the assertion the memory of the Eaton prior art reference is used by a single processor.

B. As to point (2), although Eaton is silent with reference to passing data between multiple processors, the Feemster explicitly teaches passing data between prcoessors (see Abstract, figure 2 Col. 5 Ln. 45 – 67, Col. 6 Ln. 16 – 30, figures 3/4/5 Col. 7 Ln. 38 – 67, Col. 8 Ln. 8 – 56).

C. As to point (3), In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, firstly, the two systems provide a common memory shared by multiple processors therefore making the two systems analogous. The Examiner does not suggest that the system of Eaton and Feemster would physically be combined to reach Applicant's invention. Examiner's point is that the idea of common memory that addressably fills upward through the highest physical address of the common memory and addressably fills downward through to a lowest physical address of the common memory is taught by Eaton.

D. As to point (4), the Eaton prior art reference explicitly teaches a common memory addressably filling upward through the a highest physical address of the common memory and addressably filling downward through to a lowest physical address of the common memory (Col. 4 Ln. 7 – 23). The fact that Eaton does not use "mailbox" to represent the addressable memory areas that grows upwards and downward does not affect the main idea of Eaton which is memory areas that grows/fills from opposite direction to towards each other in a common memory.

Conclusion

36. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles E Anya whose telephone number is (703) 305-3411. The examiner can normally be reached on M-F (8:30-6:00) First Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, An Meng-Ai can be reached on (703) 305-9678. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Charles E Anya
Examiner
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